What is claimed is:

1. A memory device comprising:

a delay locked loop (DLL) for generating an internal clock signal based on an external clock signal, the DLL keeping the external and internal clock signals synchronized by performing a synchronization operation; and

a DLL controller connected to the DLL for activating a DLL control signal during a test mode of the memory device to prevent the DLL from performing the synchronization operation during the test mode.

2. The memory device of claim 1 further comprising a plurality of memory cells for storing data.

3. The memory device of claim 2, wherein during the test mode, the memory cells are activated in preparation for subsequent access to the memory cells.

4. The memory device of claim 2, wherein during the test mode, the memory cells are accessed for reading the data stored in the memory cells.

5. The memory device of claim 2, wherein during the test mode, the memory cells are refreshed to ensure the memory cells retain valid data values.

6. The memory device of claim 1, wherein the DLL includes:

a phase detector for comparing the external and internal clock signal to activate a shifting signal when the external and internal clock signals are not synchronized; and

a shift register for performing a shifting operation based on the shifting signal to keep the external and internal clock signals synchronized.

7. The memory device of claim 6, wherein the DLL controller includes:

a test mode select input for receiving a select signal during the test mode;

a test mode control input for receiving control signal during the test mode; and

an output connected to the DLL for providing the DLL control signal, wherein during the test mode, the activation of the DLL control signal is based on control signal and in responding to the select signal.

8. A memory device comprising:

a delay locked loop (DLL) for applying a delay to an external clock signal to generate an internal clock signal, the DLL adjusting the delay to keep the external and internal clock signals synchronized; and

a DLL controller for activating a DLL control signal during a test mode of the memory device to prevent the DLL from adjusting the delay during the test mode.

9. The memory device of claim 8 further comprising a plurality of memory cells, wherein during the test mode, the memory cells are activated in preparation for subsequent access to the memory cells.

10. The memory device of claim 8 further comprising a plurality of memory cells, wherein during the test mode, the memory cells are accessed for reading data stored in the memory cells.

11. The memory device of claim 8 further comprising a plurality of memory cells, wherein during the test mode, data in stored in the memory cells are refreshed to ensure the memory cells retain valid data values.

12. The memory device of claim 8, wherein the DLL includes:

a phase detector for comparing the external and internal clock signals to activate a shifting signal when the external and internal clock signals are not synchronized; and

a shift register for adjusting the delay based on the shifting signal to keep the external and internal clock signals synchronized.

13. The memory device of claim 8, wherein the DLL controller includes:

a test mode select input for receiving a select signal during the test;

a test mode control input for receiving control signal during the test; and

an output connected to the DLL for providing the DLL control signal, wherein during the test mode, the activation of the DLL control signal is based on control signal and in responding to the select signal.

14. A memory device comprising:

a plurality of inputs for receiving a plurality of input signals and an external clock signal;

a delay locked loop (DLL) for generating an internal clock signal based on the external clock signal, the DLL performing a shifting operation to keep the external and internal clock signals synchronized;

a decode circuit for activating a test mode signal based on certain combination of the input signals to initiate a test mode of the memory device; and

a DLL controller for activating a DLL control signal to disable the shifting operation during the test mode.

15. The memory device of claim 14 further comprising a plurality of memory cells, wherein during the test mode, the memory cells are being activated for subsequent access to the memory cells.

16. The memory device of claim 14, wherein the DLL includes a delay line having a plurality of delay stages connected in series, wherein a number of the delay stages applies an amount of delay to the external clock signal to generate the internal clock signal.

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17. The memory device of claim 14, wherein the DLL further includes:

a phase detector for comparing the external and internal clock signals to activate a shifting signal when the external and internal clock signals are not synchronized; and

a shift register for adjusting the amount of delay based on the shifting signal to keep the external and internal clock signals synchronized.

18. The memory device of claim 14, wherein the DLL controller includes:

a test mode select input for receiving a select signal during the test;

a test mode control input for receiving control signal during the test; and

an output connected to the DLL for providing the DLL control signal, wherein during the test mode, the activation of the DLL control signal is based on control signal and in responding to the select signal.

19. A memory device comprising:

a delay line for applying an amount of delay to the external clock signal to generate the internal clock signal;

a phase detector for comparing the external and internal clock signals to activate a shifting signal when the external and internal clock signals are not synchronized;

a shift register for performing a shifting operation to adjust the amount of delay based on the shifting signal to keep the external and internal clock signals synchronized;

a test mode select input for receiving a test select signal;

a test mode control input for receiving test control signal; and

an output connected to the phase detector providing the DLL control signal, wherein the DLL control signal deactivates the shifting operation when the test select and test control signals are activated during a test mode.

20. The memory device of claim 19, wherein the phase detector includes:

input latches to receive the external and a feedback signal, the feedback signal being a delayed version of the internal clock signal, the input latches provide a first and second phase signals;

logic circuit connected to the input latches to receive the phase signals to generate pre-shifting signals;

output latches for activating shifting signals based on the pre-shifting signals when the external and internal clock signals are not synchronize; and

and a shifting signal control circuit for deactivating the shifting signal during the test mode.

21. A system comprising:

a processor; and

a memory device connected to the processor, the memory device including:

a delay locked loop (DLL) for generating an internal clock signal based on an external clock signal, the DLL keeping the external and internal clock signals synchronized by performing a synchronization operation; and

a DLL controller connected to the DLL for activating a DLL control signal during a test mode of the memory device to prevent the DLL from performing the synchronization operation during the test mode.

22. The system of claim 21 further comprising a plurality of memory cells for storing data.

23. The system of claim 21, wherein during the test mode, the memory cells are activated in preparation for subsequent access to the memory cells.

24. The system of claim 21, wherein during the test mode, the memory cells are accessed for reading the data stored in the memory cells.

25. The system of claim 21, wherein during the test mode, the data in the memory cells are refreshed to ensure the memory cells retain valid data values.

26. A system comprising:

a processor; and

a memory device connected to the processor, the memory device including:

a delay locked loop (DLL) for applying a delay to an external clock signal to generate an internal clock signal, the DLL adjusting the delay to keep the external and internal clock signals synchronized; and

a DLL controller for activating a DLL control signal during a test mode of the memory device to prevent the DLL from adjusting the delay during the test mode.

27. The system of claim 26 further comprising a plurality of memory cells arranged in rows and columns.

28. The system of claim 26, wherein in the test mode, a row of the memory cells is activated in preparation for subsequent access to the memory cells.

29. The system of claim 26, wherein in the test mode, a column of the memory cells is activated in preparation for subsequent access to the memory cells.

30. A method of testing a delay locked loop (DLL) in a memory device, the method comprising:

activating a test mode signal during a test mode;

activating a DLL control signal when the test mode signal is activated; and

disabling the DLL with the DLL control signal such that the DLL does not perform a synchronization operation during the test mode, wherein the synchronization operation synchronizes an external clock signal and an internal clock signal.

31. The method of claim 30, wherein activating a test mode signal includes applying a combination of input signals to inputs of the memory device.

32. The method of claim 30, wherein activating a DLL control signal includes asynchronously activating the DLL control signal.

33. The method of claim 30, wherein activating a DLL control signal includes activating the DLL control signal independently from cycle time of the external clock signal.

34. A method of testing a memory device, the method comprising:

activating a test mode signal during a test mode;

generating an internal clock signal based on an external clock signal during the test mode;

performing a synchronization operation to keep the external and internal clock signals synchronized;

activating a test mode control signal; and

activating a DLL control signal based on the test mode control signal to disable the synchronization operation during the test mode.

35. The method of claim 34, wherein generating an internal clock signal includes delaying the external clock signal.

36. The method of claim 34, wherein activating a DLL control signal includes asynchronously activating the DLL control signal.

37. The method of claim 34, wherein activating a DLL control signal includes

activating the DLL control signal independently from cycle time of the external clock signal.

38. A method of testing a memory device, the method comprising:

activating a test mode signal during a test mode;

applying a delay to an external clock signal to generate an internal clock signal during the test mode;

adjusting the delay to keep the external and internal clock signals synchronized;

activating a test mode control signal; and

activating a DLL control signal based on the test mode control signal to stop adjusting the delay during the test mode.

39. The method of claim 38 further includes:

generating a data output signal based on the internal clock signal during the test mode when the test mode control signal is not activated; and

recording the signal relationship between the external signal and the data output signal when test mode control signal is not activated.

40. The method of claim 39 further includes:

generating a data output signal based on the internal signal during the test mode when the test mode control signal is activated; and

recording the signal relationship between the external signal and the data output signal when the test mode control signal is activated.

41. The method of claim 40 further includes comparing the signal relationship between the external clock and output data signals before and after the test mode control signal is activated.

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